Accelerator Series FPGAs – ACT™ 3 Family

Features

- Up to 10,000 Gate Array Equivalent Gates (up to 25,000 equivalent PLD Gates)
- Highly Predictable Performance with 100% Automatic Placement and Routing
- 7.5 ns Clock-to-Output Times
- Up to 250 MHz On-Chip Performance
- Up to 228 User-Programmable I/O Pins
- Four Fast, Low-Skew Clock Networks
- More than 500 Macro Functions
- Replaces up to twenty 32 macro-cell CPLDs
- Replaces up to one hundred 20-pin PAL® Packages
- Up to 1153 Dedicated Flip-Flops
- VQFP, TQFP, BGA, and PQFP Packages
- Nonvolatile, User Programmable
- Fully Tested Prior to Shipment
- 5.0V and 3.3V Versions
- Optimized for Logic Synthesis Methodologies
- Low-power CMOS Technology

Device	A1415	A1425	A1440	A1460	A14100
Capacity					
Gate Array Equivalent Gates	1,500	2,500	4,000	6,000	10,000
PLD Equivalent Gates	3,750	6,250	10,000	15,000	25,000
TTL Equivalent Packages (40 gates)	40	60	100	150	250
20-Pin PAL Equivalent Packages (100 gates)	15	25	40	60	100
Logic Modules	200	310	564	848	1,377
S-Module	104	160	288	432	697
C-Module	96	150	276	416	680
Dedicated Flip-Flops[1]	264	360	568	768	1,153
User I/Os (maximum)	80	100	140	168	228
Packages[2] (by pin count)					
CPGA	100	133	175	207	257
PLCC	84	84	84	—	—
PQFP	100	100, 160	160	160, 208	—
RQFP	—	—	—	—	208
VQFP	100	100	100	—	—
TQFP	—	—	176	176	—
BGA	—	—	—	225	313
CQFP	—	132	—	196	256
Performance[3] (maximum, worst-case commercial)					
Chip-to-Chip[4]	108 MHz	108 MHz	100 MHz	97 MHz	93 MHz
Accumulators (16-bit)	63 MHz	63 MHz	63 MHz	63 MHz	63 MHz
Loadable Counter (16-bit)	110 MHz	110 MHz	110 MHz	110 MHz	105 MHz
Prescaled Loadable Counters (16-bit)	250 MHz	250 MHz	250 MHz	200 MHz	200 MHz
Datapath, Shift Registers	250 MHz	250 MHz	250 MHz	200 MHz	200 MHz
Clock-to-Output (pad-to-pad)	7.5 ns	7.5 ns	8.5 ns	9.0 ns	9.5 ns

Notes:

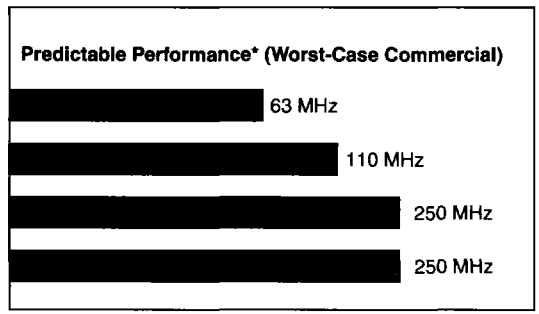
1. *One flip-flop per S-Module, two flip-flops per I/O-Module.*
2. *See product plan on page 1-180 for package availability.*
3. *Based on A1415A-3, A1425A-3, A1440B-3, A1460B-3, and A14100B-3.*
4. *Clock-to-Output + Setup*

Description

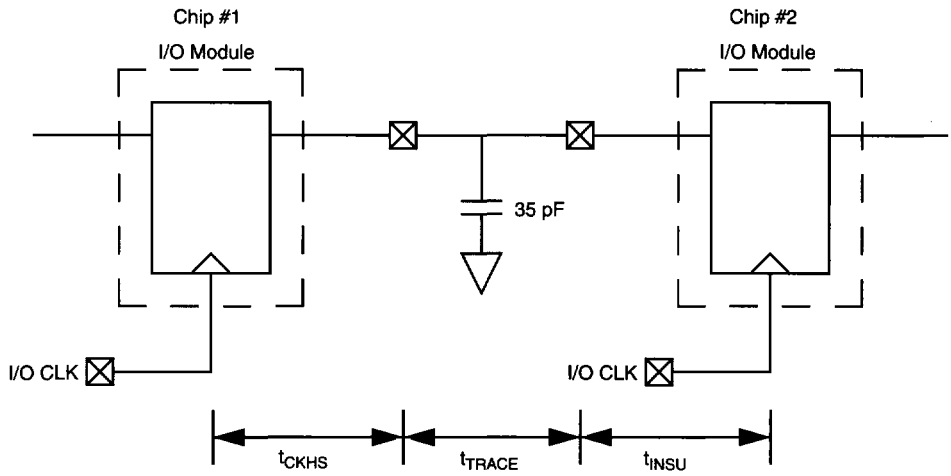
Actel's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high perfomance, PCI compliant programmable solution capable of 250 MHz on-chip performance and 7.5 nanosecond clock-to-output, with capacities spanning from 1,500 to 10,000 gate array equivalent gates. For further information regarding PCI compliance of ACT 3 devices, see "Accelerator Series FPGAs—ACT 3 PCI Compliant Family."

The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Actel's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 7.5 nanosecond clock-to-out times. The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output enables.

The ACT 3 family is supported by Actel's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing anlaysis, user programming, and debug and diagnostic probe capabilities. The Designer Series is supported on the following platforms: 486/Pentium class PC's, Sun®, and HP®, workstations. The software provides CAE interfaces to Cadence, Mentor Graphics®, OrCAD™ and Viewlogic®, design environments. Additional platforms are supported through Actel's Industry Alliance Program, including DATA I/O (ABEL FPGA) and MINC.

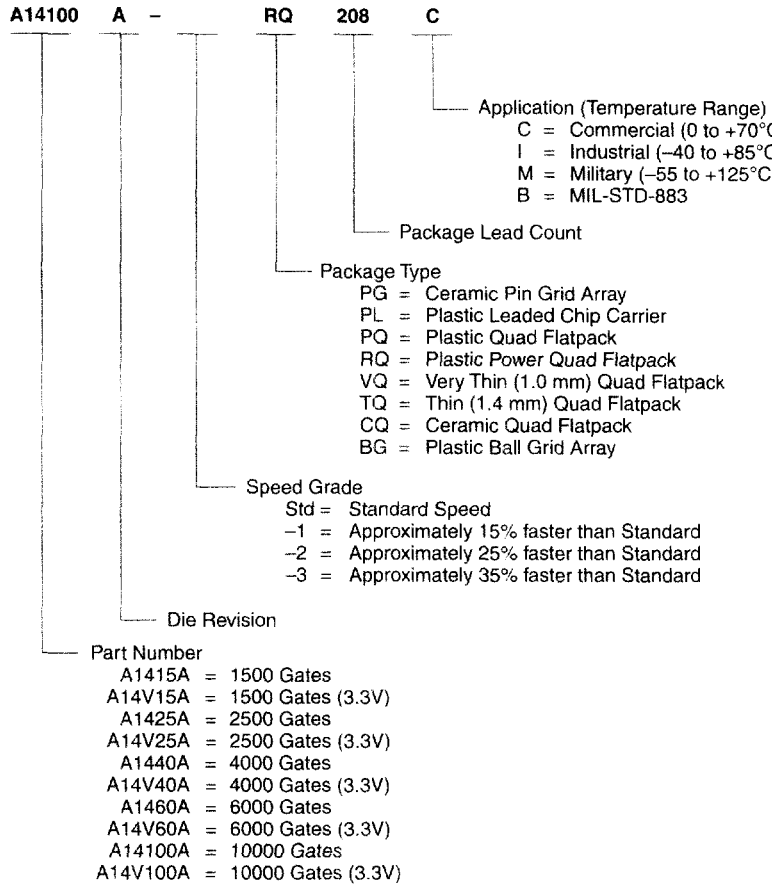


System Performance Model



Chip-to-Chip Performance (Worst-Case Commercial)					
	t_{CKHS}	t_{TRACE}	t_{INSU}	Total	MHz
A1425A-3	7.5	1.0	1.8	10.3 ns	97
A1460A-3	9.0	1.0	1.3	11.3 ns	88

Ordering Information



A complete product description is available from the Actel Web site (www.actel.com), the Digital Library CD or an Actel Representative.